

FAMES Pilot Line In *Nature Reviews Electrical Engineering*

GRENOBLE, FRANCE – Feb. 7, 2025 – The FAMES Pilot Line offers a complete set of technologies to develop innovative chip architectures. FAMES will open new research avenues for enhancing performance and lowering power consumption for mixed-signal circuits – and strengthening European sovereignty in microelectronics, CEA-Leti reported in a recent article in [Nature Reviews Electrical Engineering](#).

The [FAMES Pilot Line](#) focuses on five sets of technologies that will enable new chip architectures:

- FD-SOI, with two new-generation nodes at 10nm and 7nm,
- Embedded non-volatile memories (eNVM) – Enhancing storage capabilities in advanced integrated circuits,
- Radio frequency (RF) components – Optimizing high-performance connectivity for next-generation wireless applications,
- Two 3D integration technologies – Enabling advanced 3D stacking and heterogeneous integration for enhanced chip functionality, and
- Small inductors to develop DC-DC converters for power-management integrated circuits (PMIC).

The new technologies will create market opportunities for low-power microcontrollers (MCU), multi-processor units (MPU), cutting-edge AI and machine-learning devices, smart data-fusion processors, RF devices, chips for 5G/6G, chips for automotive markets, smart sensors and imagers, trusted chips and new space components.

FAMES will provide open access to stakeholders across Europe and partner countries. Researchers, SMEs, and industrial companies can leverage the pilot line for circuit testing, design evaluation, and new technology development. The annual open calls, the first one to be launched in March, will enable interested stakeholders to engage with the pilot line, and contribute to Europe’s expanding the semiconductor ecosystem.

“All technologies developed in the FAMES Pilot Line will enable new chip architectures delivering robust performance enhancements and substantial efficiency gains, fulfilling users’ requirements and sustainably supporting the massive digitalization of our society,” said Jean-René Lèquepeys, deputy director and CTO of CEA-Leti and lead author of the article.

“It also will drive eco-friendly practices by prioritizing resource optimization, advocating for a circular economy, and minimizing waste across the entire technological process, from chip design to manufacturing,” he explained.

The FAMES consortium that will support the initiative includes: the pilot line coordinator, [CEA-Leti](#) (France), [imec](#) (Belgium), [Fraunhofer](#) (Germany), [Tyndall](#) (Ireland), [VTI](#) (Finland), [CEZAMAT WUT](#) (Poland), [UCLouvain](#) (Belgium), [Silicon Austria Labs](#) (Austria), [SiNANO Institute](#) (France), [Grenoble INP](#) (France) and the [University of Granada](#) (Spain).

The project’s €830 million, five-year budget is jointly funded by the EU and participating member states.

About FAMES

For more about the FAMES partners, [click here](#).

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