

FAMES Pilot Line Inaugurated After Delivering First Validated Technical Results

*New Cleanroom Is a World-Class Facility
That Will Host State-of-the-Art 300mm Semiconductor Equipment*

GRENOBLE, France — Jan. 30, 2026 — The FAMES Pilot Line was officially inaugurated today—two years after it began, now delivering validated technical results across advanced FD-SOI, RF, embedded non-volatile memories, 3D integration technologies, and Power Management ICs. Those results, produced on a 300 mm line and reported at leading international conferences, confirm that the European tech-sovereignty initiative is already operating as a working European semiconductor capability.

Today's inauguration, attended by more than 350 people, marks the launch of a cleanroom extension at CEA-Leti's Grenoble site. The open-access feature of the pilot line makes the FAMES technologies accessible primarily, but not exclusively, to European startups, SMEs, industrial groups, and research organizations seeking to prototype, qualify, and de-risk advanced semiconductor technologies before industrial deployment. The initiative is coordinated by the CEA.

Technological momentum

Since entering operation, the pilot line has generated concrete advances across its core domains, spanning substrates, embedded ferroelectric non-volatile memories, advanced FD-SOI, 3D integration, high performance RF passive components—areas critical to next-generation chips.

“The breakthrough technologies developed within FAMES are intended to support future generations of sub-10 nm FD-SOI chips, enabling high-performance and low-power components for Europe,” said Jean-René Lèquepeys, deputy director and CTO of CEA-Leti. “Scaling down the FD-SOI technology to 10 and 7nm will bring significant chip performance improvements compared to current nodes, in density, power consumption, speed and radio-frequency behavior.”

Among the most recent milestones, CEA-Leti recently presented results at IEDM 2025 demonstrating fully functional 2.5 V SOI CMOS devices fabricated at a thermal budget of 400 °C. Achieving performance comparable to conventional high-temperature CMOS, the work removes a key barrier to large-scale 3D sequential integration and enables dense multi-tier chip architectures compatible with advanced back-end processes—one of the central technical objectives of FAMES.

Ultra-efficient ecological systems

With 2,000 m² of cleanroom space, the new facility expands CEA-Leti's cleanroom space to 14,000 m². It will house more than 80 state-of-the-art 300mm cleanroom tools. Two basement levels help manage complex technical installations, and a five-meter ceiling height accommodates large equipment. In addition, very low vibration levels and dedicated electrical back-up systems will ensure uninterrupted operation.

In addition to housing some of the semiconductor industry's most specialized and sophisticated tools, the facility has been equipped with systems and processes enabling advanced optimization of its environmental footprint.

The building incorporates high-performance insulation requirements and will enable the implementation of waste-energy recovery solutions (residual heat recovery).

Following the French *France 2030* NextGen project, which was launched in 2022, the FAMES pilot Line project provided additional momentum in 2023 under the EU Chips Act. These two initiatives were designed to shorten the path from research to industrial readiness by providing a leading edge, open-access environment for technology innovation.

'The role FAMES is meant to play'

“The fact that results are already being published and validated internationally underscores the role FAMES is meant to play,” said Dominique Noguét, vice president at CEA-Leti and coordinator of the pilot line. “This is not a future manufacturing line. It is an operational platform where advanced technologies are being matured, demonstrated, and prepared for transfer to industry.”

With a total investment of €830 million, co-funded by the European Commission under the Chips Act and by participating Member States, FAMES brings together 11 partners across eight countries. Its objective is to reduce the time between research and industrialization, while strengthening Europe’s technological autonomy in semiconductor domains that underpin strategic sectors including automotive, telecommunications, edge AI, industrial systems, health, space, and cybersecurity.

By inaugurating a pilot line that is already producing validated results, FAMES exemplifies the lab-to-industry model at the core of Europe’s semiconductor strategy—providing industry with access to mature technologies, proven processes, and a direct path toward future manufacturing.

'Fully aligned with the ambition of the Chips Act'

“With the inauguration of FAMES, the CEA is providing Europe with a unique capability to accelerate the maturation of strategic technologies and their transfer to industry,” said Anne-Isabelle Etienne, the Director General of the CEA. “This success illustrates the strength of our ‘lab to industry’ model, based on scientific excellence and close operational relationships with industrial players. It is fully aligned with the ambition of the Chips Act and is already preparing the next step: consolidating, with our partners, a long-term European dynamic to secure innovation and technological sovereignty in microelectronics.”

About FAMES Pilot Line

FAMES (FD-SOI Pilot Line for Applications with embedded non-volatile Memories, RF, 3D Integration & PMIC, to ensure European Sovereignty) gathers leading RTOs and academic partners to develop five key technologies and an eco-innovation program that will enable new chip architectures. The project includes an open access program to enable semiconductor stakeholders to gain access to the Pilot Line and the FAMES technologies, and a comprehensive training program.

Visit <https://fames-pilot-line.eu/>

In addition to the pilot line coordinator, France-based [CEA-Leti](#), the FAMES consortium includes [imec](#) (Belgium), [Fraunhofer](#) (Germany), [VTT](#) (Finland), [CEZAMAT WUT](#) (Poland), [Tyndall](#) (Ireland), [Silicon Austria Labs](#) (Austria), [UCLouvain](#) (Belgium), [Grenoble INP](#) (France), [SiNANO Institute](#) (France) and the [University of Granada](#) (Spain).

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