FAMES Pilot Line & SiNANO Institute to Present FAMES' Latest Technical Results at ESSERC 2026 in Palma de Mallorca, Spain

Sept. 7, 2026 workshop will feature comprehensive technical update, spanning advanced FD-SOI nodes, embedded memories, RF filters, 3D integration and power management ICs

GRENOBLE, France – July 23, 2026 – The FAMES Pilot Line and SiNANO Institute will host a joint half-day workshop, "FD-SOI Pilot Line Insights and Perspective," on Sept. 7 at ESSERC 2026, the European Solid-State Electronics Research Conference, in Palma de Mallorca, Spain. The session will present the latest in-depth technical results from the pilot line.

Launched two and a half years ago as one of five pilot lines of the Chips Joint Undertaking under the European Chips Act, FAMES has delivered significant technical results across its five core technologies: advanced FD-SOI nodes, embedded non-volatile memories (eNVM), RF passive components, 3D integration and power-management ICs (PMIC). The ESSERC presentations will share FAMES' most comprehensive workshop material to date.

'Deep Dive Into Key Technologies'

"The results we're presenting at ESSERC — from performance boosters for the 10nm node to the first millimeter-wave RF circuits fabricated in a full 3D sequential process — will be a detailed, deep dive into key technologies developed by FAMES and an opportunity for participants to meet and network with some of our top experts," said FAMES Coordinator and CEA-Leti Vice President Dominique Noguet.

As the leading European nanoelectronics academic and scientific association, SiNANO Institute is a member of the 11-partner FAMES consortium. It brings together Europe's nanoelectronics community to create research agendas, foster collaboration and accelerate innovation.

"This joint workshop reflects SiNANO's mission by creating a bridge between the FAMES Pilot Line and the wider research and industrial ecosystem, ensuring that breakthrough developments in FD-SOI, embedded memories, RF technologies, power management ICs and 3D integration can deliver impact across Europe," noted Giorgos Fagas, director of the institute and director of strategic development at Tyndall National Institute, also a consortium member.

Workshop Presentations

The FAMES Pilot Line: *Opportunities for the Next Generation of Chips*, Dominique Noguet
An overview of the €830 million initiative's five technology programmes and of how semiconductor stakeholders can gain access to the pilot line and its technologies.

SiNANO Institute: *Connecting Europe's Nanoelectronics Community*, Giorgos Fagas
How the European nanoelectronics association is linking the FAMES Pilot Line to the wider research and industrial ecosystem.

Next Generations of FD-SOI Technology for Low-Power and RF Applications, Thierry Poiroux, CEA-Leti, and Valeriya Kilchytska, UCLouvain
A detailed look at the 10nm FD-SOI technology developed in FAMES — designed to be 50 percent more power-efficient at constant speed, or 30 percent faster at a given power, than 22nm — and the performance boosters in the transistor architecture that make the leap possible. The second part shows how FD-SOI specificities such as local back biasing can be exploited at the circuit level, tuning different parts of a chip for high performance or extremely low leakage.

Achievements FAMES Already Produced for the Development of Embedded Non-Volatile Memories in Europe, Gabriel Parès, CEA-Leti
A midterm status report on the four eNVM flavors — OxRAM, FeRAM, MRAM and BEOL Fe(M)FET — an essential add-on to FD-SOI platforms at 10nm and 7nm, where flash no longer scales. Results span MRAM stochasticity as an entropy source for hardware security to FeRAM/FeFET as candidates to replace SRAM and eDRAM in last-level cache (>10^{11} endurance, 10ns latency, <100 fJ/bit).

Reliable RRAM-Based Physically Unclonable Functions for Energy-Efficient Hardware Security, Piotr Wiśniewski, CEZAMAT, Warsaw University of Technology
A view on how the intrinsic stochastic variability of resistive switching generates unique cryptographic signatures for authentication and secure key generation, with a focus on response reproducibility and an optimized RRAM control scheme. RRAM's non-volatile, CMOS-compatible nature enables robust, low-power root-of-trust primitives for next-generation secure IoT, embedded and edge computing.

Solidly Mounted Lithium Niobate Bulk Acoustic Wave Filters for the FR3 Range, Alexandre Reinhardt, CEA-Leti
A presentation on 6GFR3 range (7–24 GHz) bandpass filters that let mobile communications share the spectrum with existing satellite and emergency services. The talk presents CEA-Leti's ongoing work to bring acoustic filters from sub-6 GHz into FR3 by leveraging single-crystal piezoelectric materials.

Advancing 3D Sequential Integration: Process Innovations and Future Applications, Daphnée Bosch, CEA-Leti
Showcasing latest 3D sequential integration advances including versatile 2.5V n- and p-type SOI MOSFETs fabricated entirely at 400°C, which overcomes critical low-temperature challenges and opens the door to large-scale industrial adoption. These results also include the first millimeter-wave RF circuits fabricated in the top tier of a full 3DSI process for 5G, with no degradation despite the close vicinity of both tiers. The presentation extends the 3DSI vision to advanced imaging and energy-efficient computing.

The Rise of Heterogeneous Integration and 3D Architectures as Key Enablers in the AI Era, Emmanuel Ollier, CEA-Leti
An explanation of why sub-2nm nodes alone can no longer meet AI's computational demands; cloud and edge-AI now call for architectures that drastically cut data movement, latency and power consumption. The talk shows how FAMES drives the advanced packaging behind them — small-pitch hybrid bonding and through-silicon via (TSV) technologies — and the novel computing and RF architectures they enable.

Small Inductors for DC-DC Converters: Power Management Integrated Circuits, Sambuddha Khan, Tyndall National Institute

Delivering Tyndall's magnetics-on-silicon platform stripline micro-inductors (5–10 nH, 20–50 MHz) with optimized CoZrTa/AlN laminated cores and quality factors above 8, integrated onto glass substrates or into silicon trenches by tether-free micro-transfer printing while preserving inductance within ±10 percent. The talk outlines the route to buried inductor-capacitor power networks in interposers and access through the FAMES ACCESS programme.

Workshop Details

"FDSOI Pilot Line Insights and Perspective"
2–5:30 p.m., Sept. 7, 2026
ESSERC 2026, Auditorium de Palma, Palma de Mallorca, Spain
Registration: www.esserc2026.org/
More information: https://fames-pilot-line.eu/meet-fames-at-esserc-2026-in-mallorca/

About FAMES Pilot Line

FAMES (FD-SOI Pilot Line for Applications with embedded non-volatile Memories, RF, 3D Integration & PMIC, to ensure European Sovereignty) gathers leading RTOs and academic partners to develop five key technologies and an eco-innovation programme that will enable new chip architectures. The project includes an open-access feature to enable semiconductor stakeholders to gain access to the FAMES Pilot Line and the FAMES technologies, and a comprehensive training programme. Visit fames-pilot-line.eu

In addition to the pilot line coordinator, France-based CEA-Leti, the FAMES consortium includes imec (Belgium), Fraunhofer (Germany), VTT (Finland), CEZAMAT WUT (Poland), Tyndall (Ireland), Silicon Austria Labs (Austria), UCLouvain (Belgium), Grenoble INP (France), SiNANO Institute (France) and the University of Granada (Spain).

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About SiNANO Institute

SiNANO Institute is the European academic and scientific association that brings together 29 top universities and research centers in semiconductor science and technologies from 16 European countries to shape research agendas, support emerging technologies and strengthen Europe's position in the global semiconductor landscape. Visit sinano.eu

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