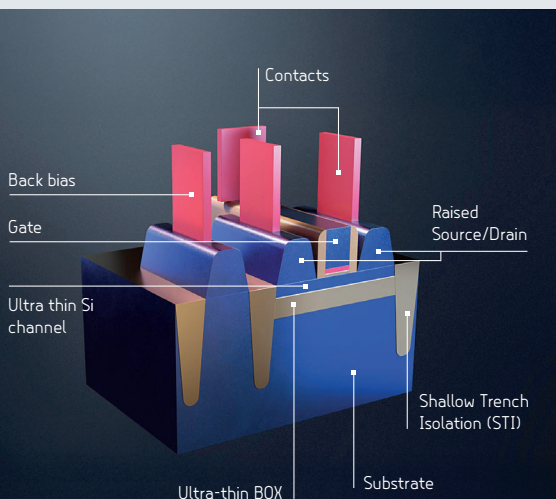
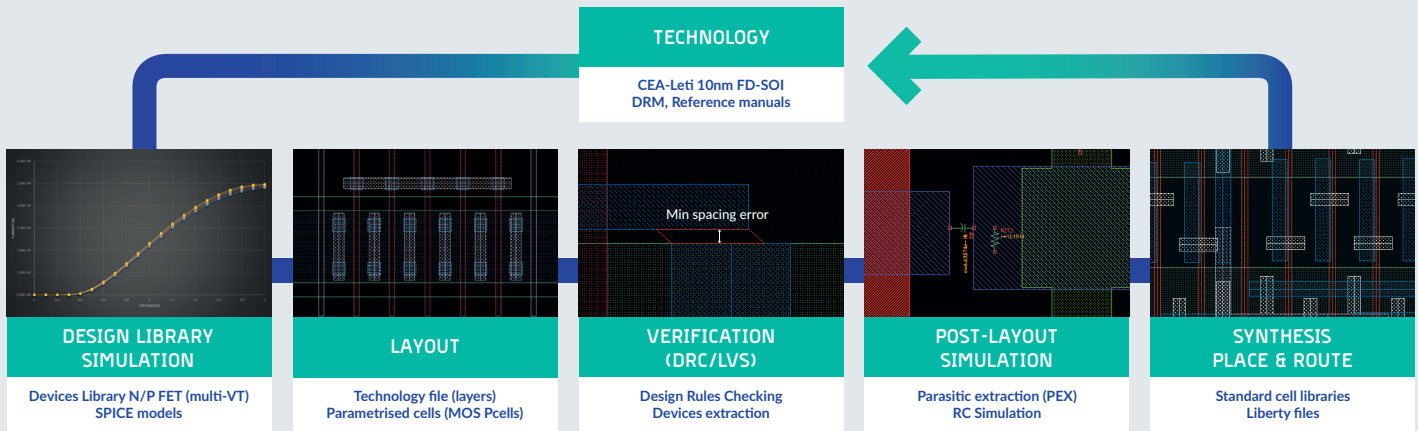


Evaluate Your Designs with FAMES' 10nm FD-SOI CMOS Technology

Based on process and device TCAD simulations combined with silicon data, this first release will help you assess digital circuits. Process assumptions are based on the most recent generations of FD-SOI technology, enabling 68nm CPP and 48nm metal pitches.



Advantages of the FD-SOI technology

- FD-SOI is a planar technology where the transistor channel is located above a thin buried oxide. Minimising the thickness of the top silicon layer above the BOX results in the absence of intrinsic charge carriers in the channel between the source and the drain contacts. Hence the name of "fully depleted" SOI. The main advantages of this very thin silicon channel is the improvement of gate control on the channel resulting in lower leakage currents and better switching characteristics.
- One of the key features of the FD-SOI technology is the ability to adjust the behaviour of transistors not only through the gate, but also by polarising the substrate underneath the device: this is called back biasing. Thanks to the ultra-thin insulator layer, back biasing can be used to dynamically adapt the circuit operating point between high performance/high speed and low power consumption/stand-by very efficiently.

<https://fames-pilot-line.eu/fd-soi/>

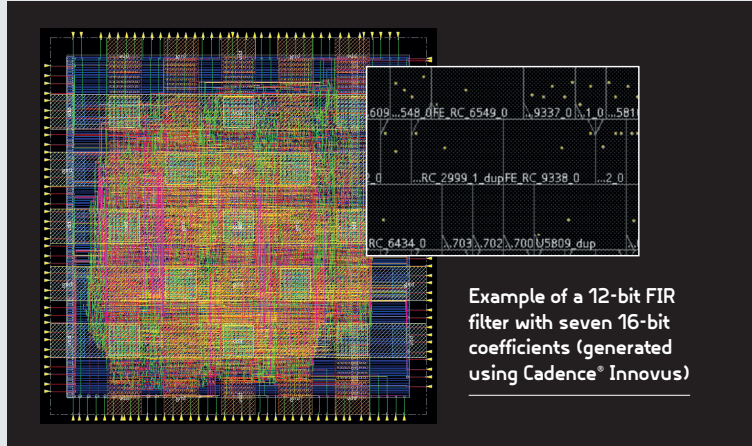
▪ PDK Specifications and Contents

- Design Rule Manual
 - Cadence® Virtuoso schematic and layout environment
 - Device library including multi-V_{th} MOSFETs
 - 4 V_{th} flavours (SLVT, LVT, RVT, HVT)
 - 2 poly-bias options for digital devices
 - SRAM transistors: pass gate, pull-up and pull-down
 - Device model library supporting multi-V_{th} solutions for SPICE simulation
- Process variability and corner support
 - Siemens® Calibre DRC/LVS deck files for physical verification
 - Synopsys® Star-RCXT parasitic extraction deck
 - Db and Lib files for digital synthesis
 - Technological LEF and QRC files for Cadence® Innovus Place&Route

- Logic Gate Libraries

CEA-Leti, in collaboration with CEZAMAT-WUT, has developed sixteen logic gate libraries, each comprising approximately 60 cells. The different logic gates correspond to combinations of the four threshold voltage levels, two poly-bias options, and two isolation schemes.

This results in two series of libraries, one for high-density and another for high-performance circuits/applications. These libraries represent approximately 1,000 logic gates, forming an essential basis for exploring, characterising, and evaluating the digital performance of the 10 nm FD-SOI node.



Access, training and technical support

- FAMES Users may obtain access to FAMES Pathfinding PDKs free of charge by signing an NDA and a Design Kit Licence Agreement. A collaborative approach will be preferred. Visit <https://fames-pilot-line.eu/open-access/>
- FD-SOI IC design training courses are regularly available through the FAMES Academy.
- FAMES Pathfinding PDK users will have access to technical support from FAMES experts and the possibility of building and publishing model case studies with one or more FAMES partners.

The FAMES Partners



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